

FIG. 1

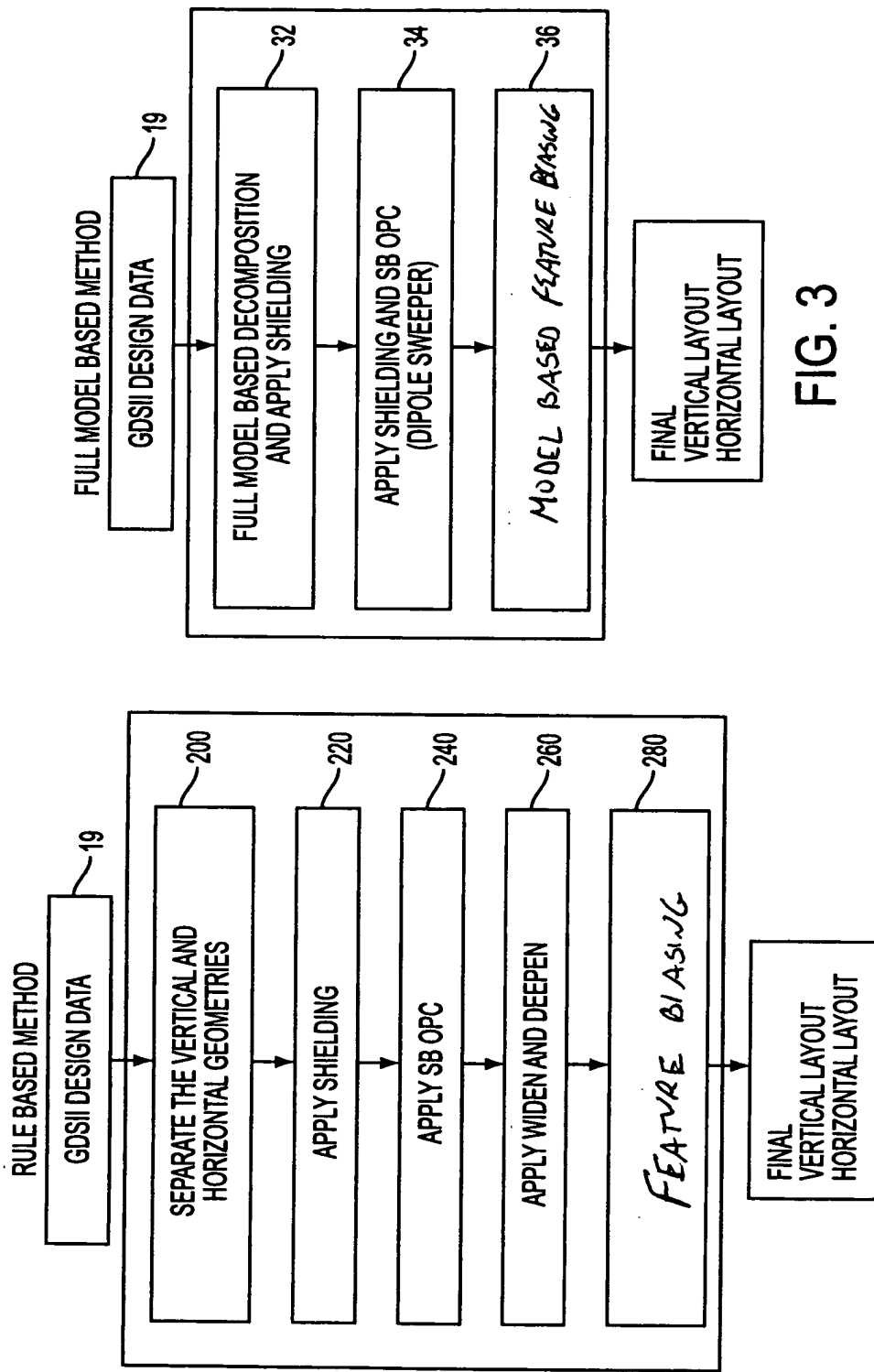


FIG. 2

FIG. 3

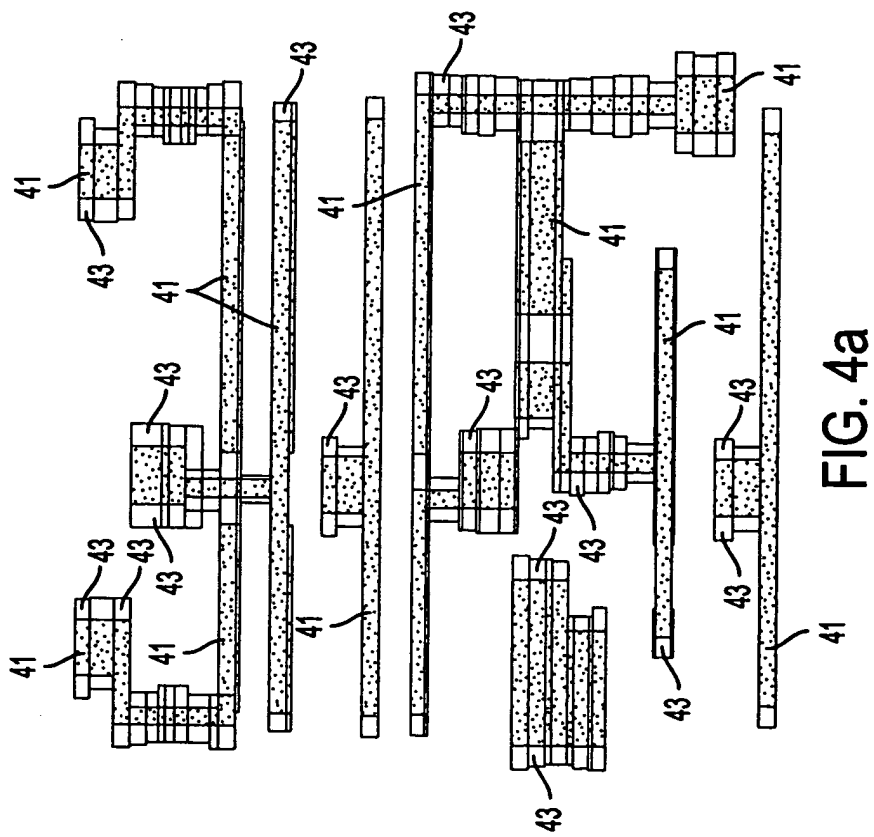


FIG. 4a

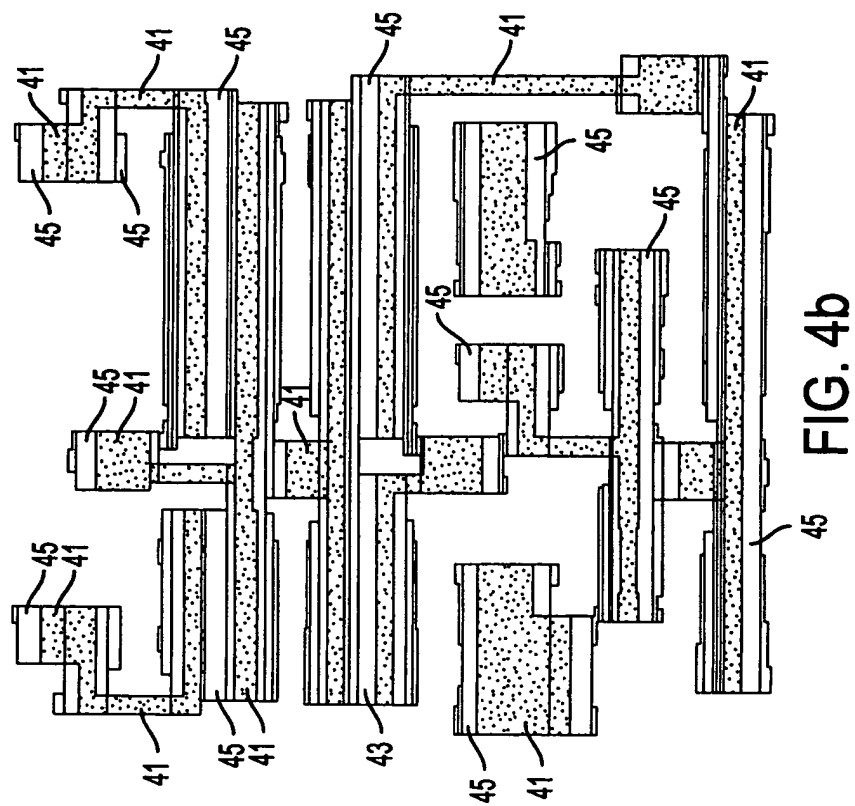


FIG. 4b

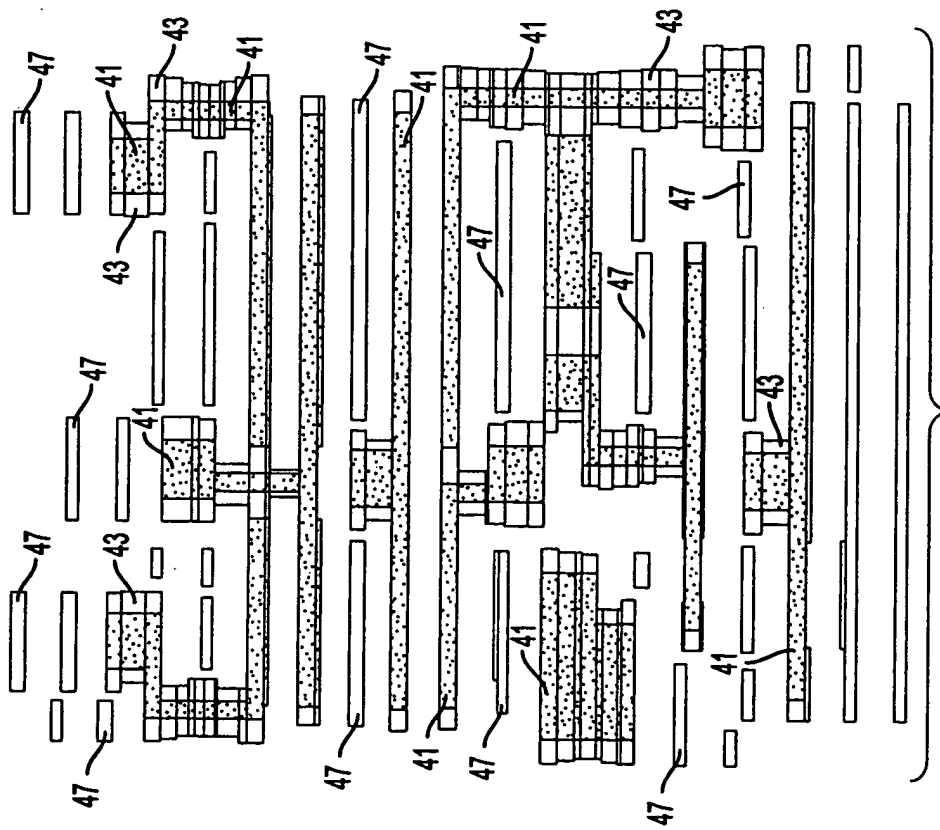


FIG. 4c

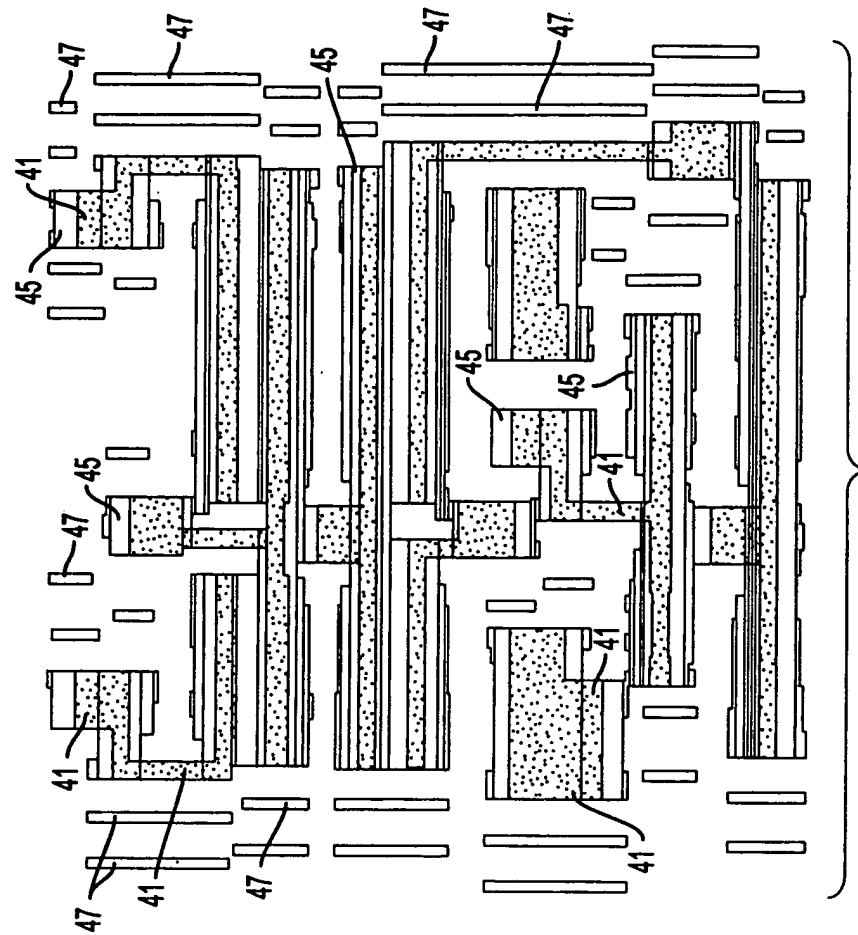


FIG. 4d

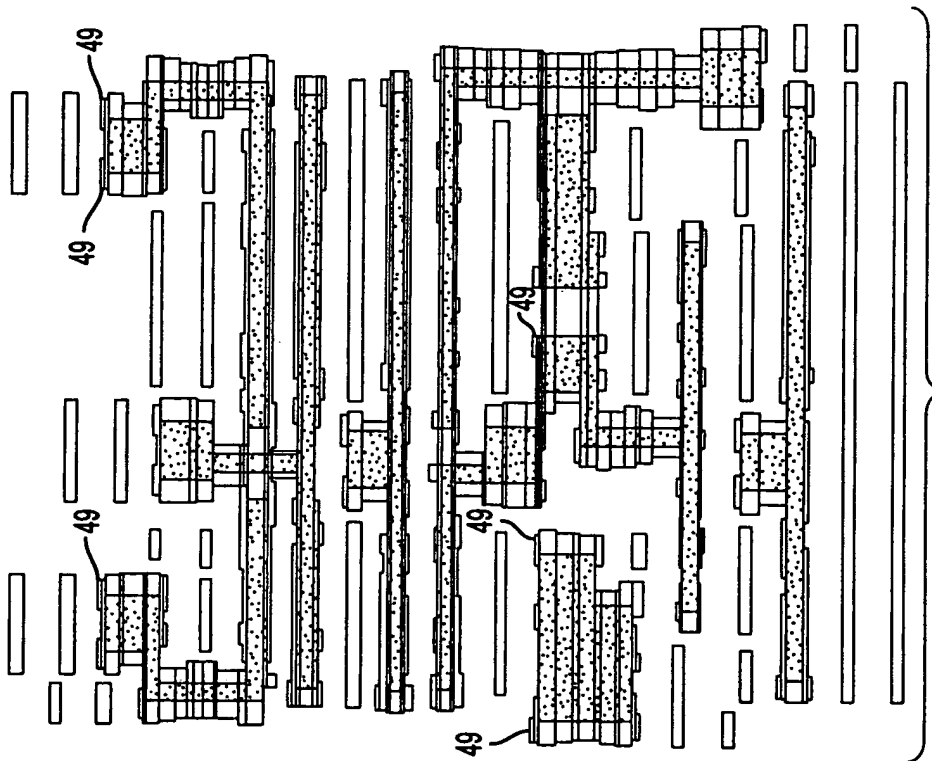


FIG. 4e

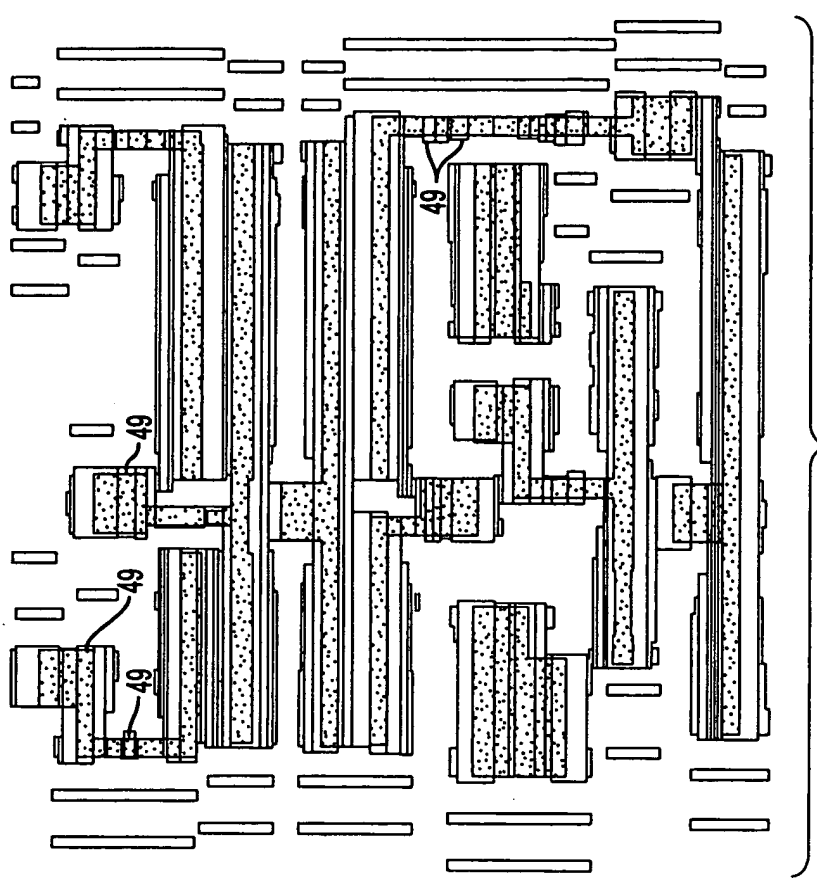
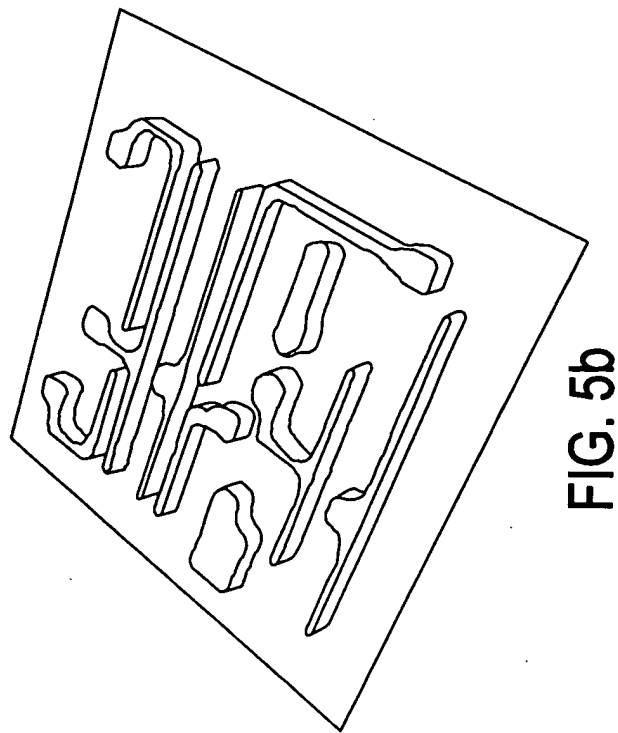
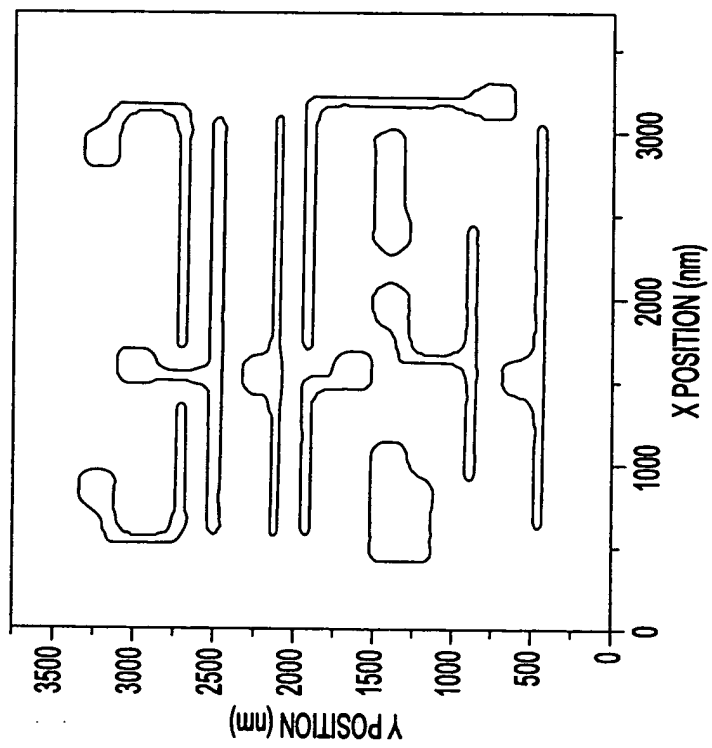


FIG. 4f



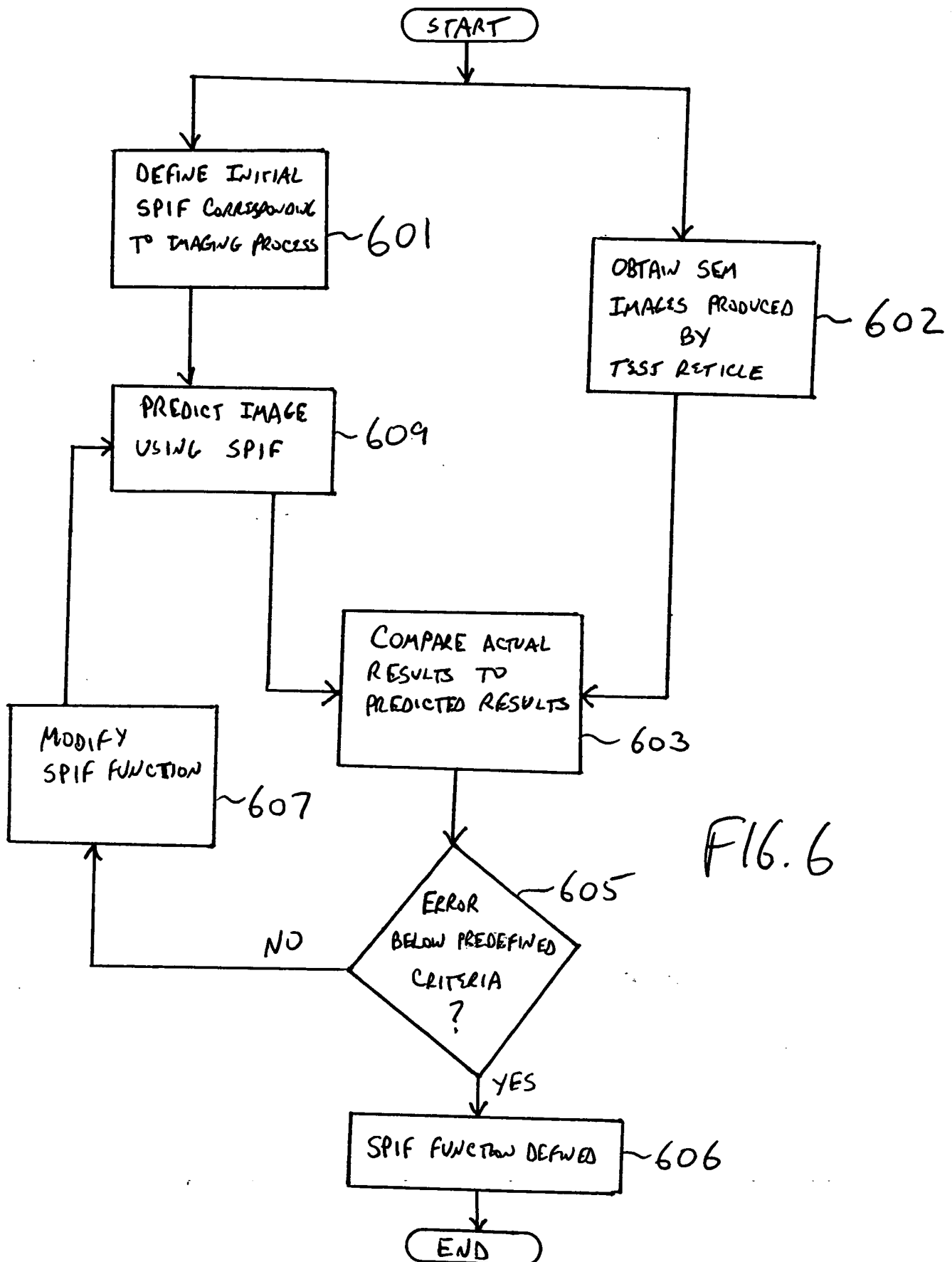
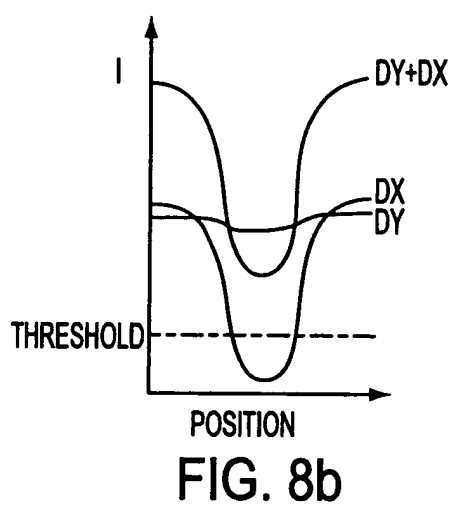
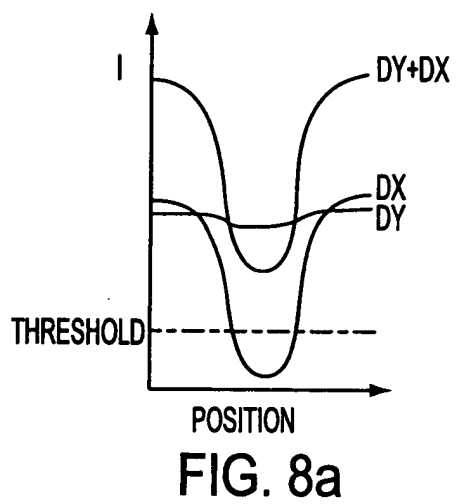
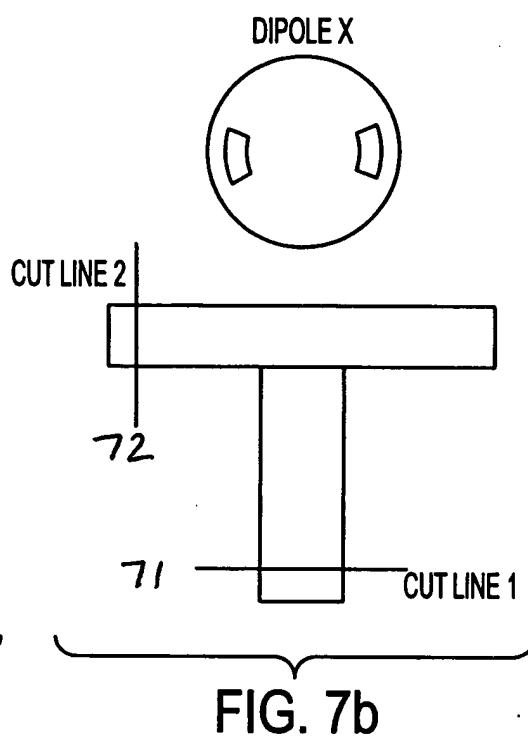
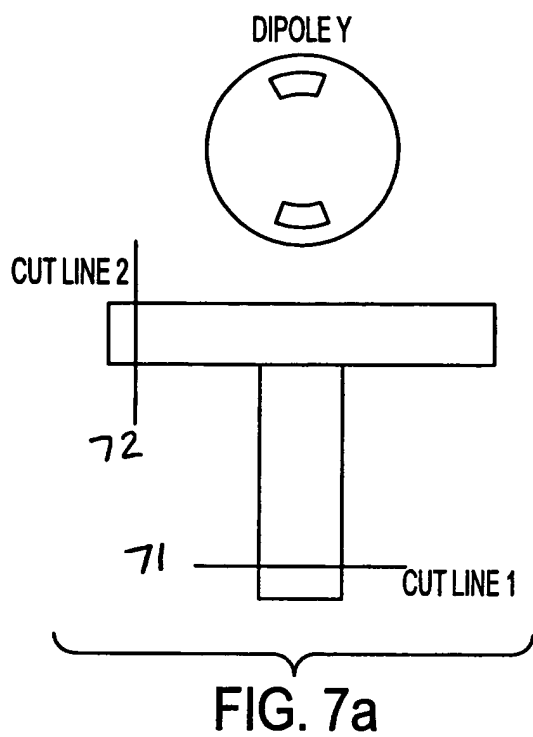


FIG. 6



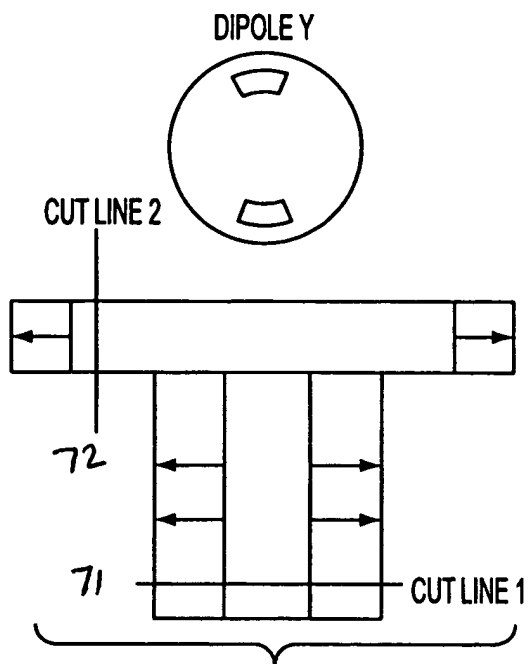


FIG. 9a

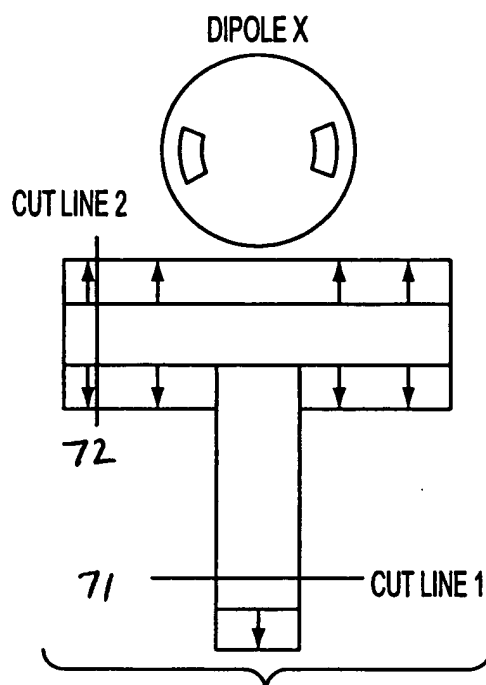


FIG. 9b

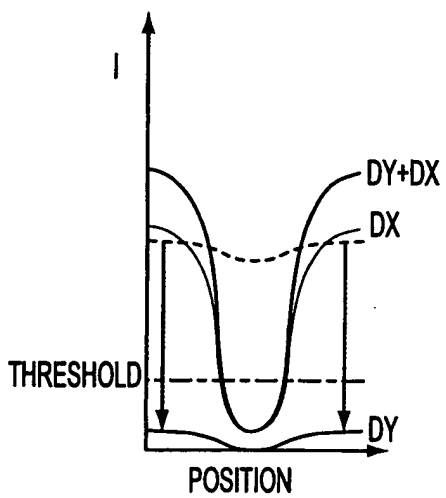


FIG. 10a

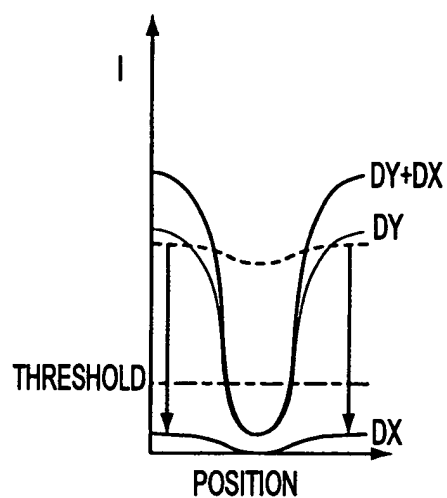
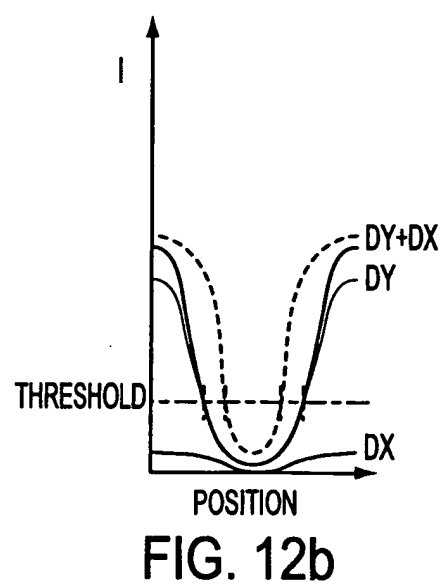
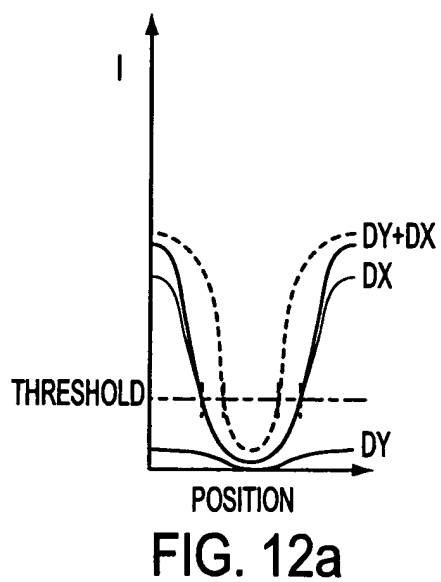
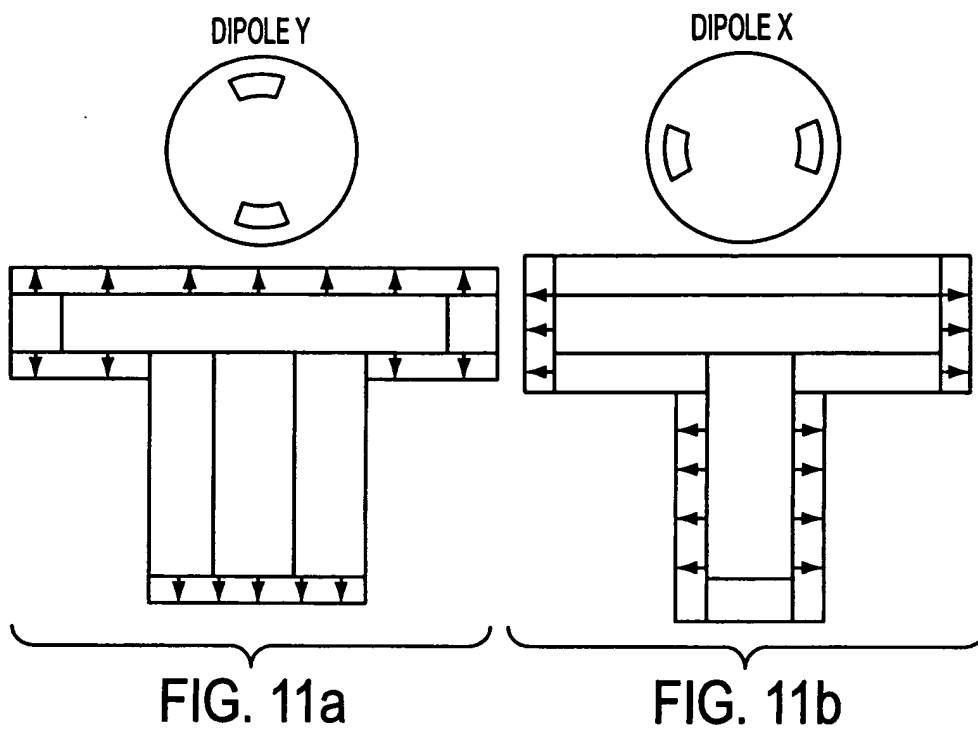


FIG. 10b



LAYOUT CONVERSION & OPC METHOD	RULE-BASED (EXISTING)	FULL MODEL METHOD
TREATMENT STEPS	4 TREATMENTS	3 TREATMENTS
JOG	SENSITIVE TO JOG	NOT SENSITIVE TO JOG
2D CORNER	NEGATIVE SERIF (WD/DP)	N/A
GATE SHRINK	READY	READY
DEVICE TYPE	MEMORY AND LOGIC NEED TO BE TREATED IN TWO PASSES	MEMORY AND LOGIC CAN BE HANDLE IN ONE PASS

FIG. 13

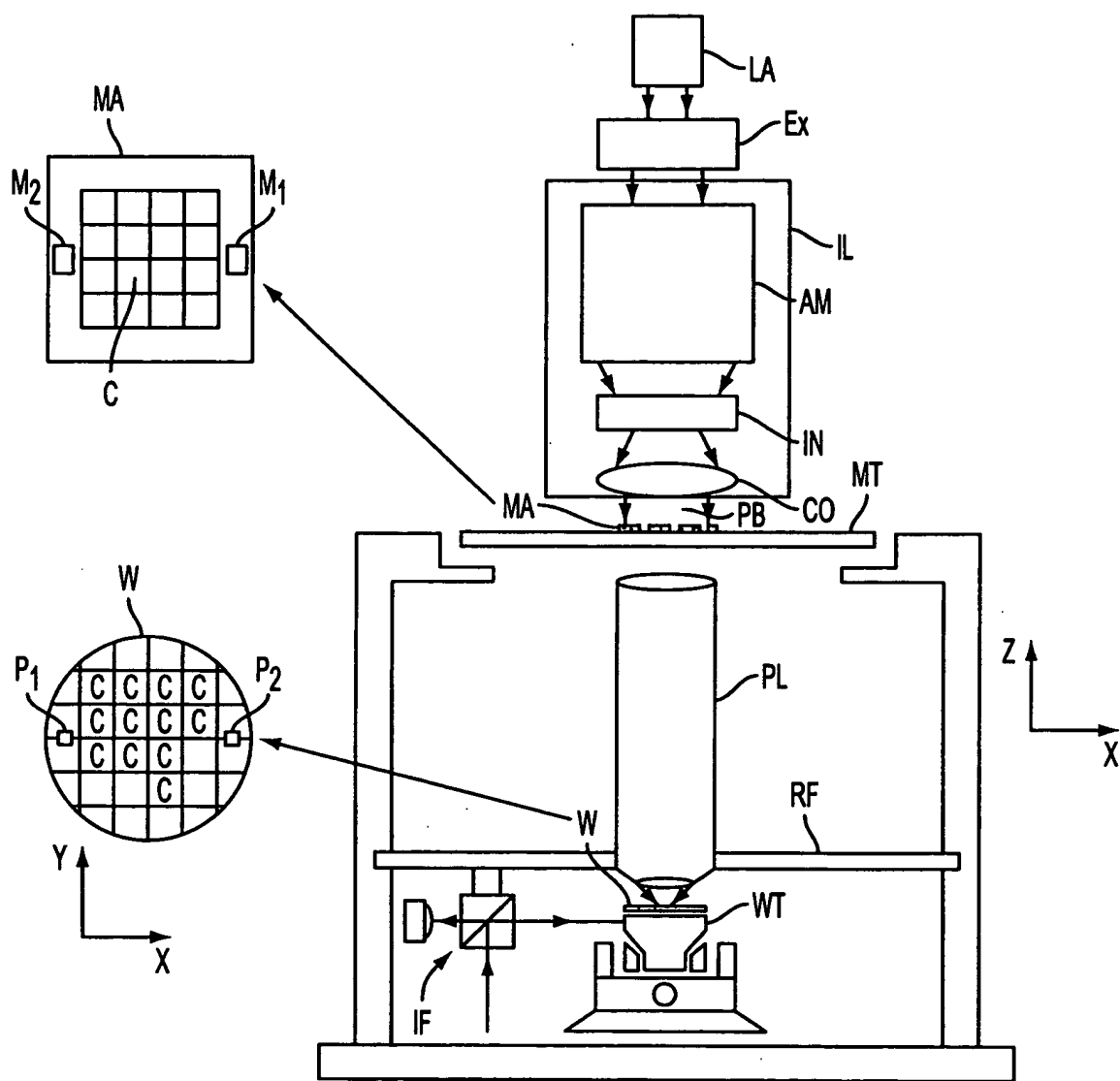


FIG. 14